Adaptive Runtime Reconfigurable Wireless Sensor Nodes Based On Dynamic Data Aggregation

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Abstract

The integration of new reconfiguration techniques in Wireless Sensor Networks (WSN) has the potential to offer improved Performance of the WSN and its applications. Proposed system can dynamically reconfigure the sensor nodes at the runtime. WSN provides the necessary information by changing the network according to the need, when the environment changes. Tree based Algorithm is used for disseminating the configuration code in WSN. Reconfigurability in a node is made possible by including a reconfigurable device Field Programmable Gate Array (FPGA). Besides Microcontroller reprogramming, this concept provides a result that brings out the reconfiguration capabilities of FPGA to provide flexibility .This shows the possibility that the reconfiguration techniques can be implemented in WSN, which may lead to the change of WSN. We can rather make the WSN generic by allocating tasks dynamically than using it as a custom made design for particular application.

Keywords: *Data Aggregation, Field Programmable Gate Array (FPGA), Wireless Sensor Networks (WSN), Reconfiguration.*

1. Introduction

Wireless Sensor Networks (WSNs) are tremendously being used in different environments to gather information or detect special events for numerous application areas including environmental ,medical, military, and transportation. Many of these applications may have some requirements which are not fully considered during design and development phase. Design modification capability is essential for a sensor network, through which it can perform new tasks assigned to it after initial deployment. In early designs wireless channels are meant for exchanging the information. Wireless channels can be used to support the new tasks assigned to the system for supporting node modification. Reconfigurable sensor Platforms offer flexibility and possibility of customization after initial deployment, it can support run time reconfiguration if the system needs.

Application Specific Integrated Circuits (ASICs) are designed for target application and hence performance of the system will be higher. Flexibility in this approach is however low because they cannot be changed after initial deployment. To achieve flexibility processor based systems were used. However performance is comparatively lower than platforms with programmable Logic and power consumption of the system is also high. Sensor Platforms with Programmable device can provide the desired characteristics of flexibility and efficiency.

In this paper we use Field Programmable Gate Array (FPGA) to achieve post manufacturing customization. Run time reconfiguration is a method to achieve the goal of reconfiguration. Flexibility is needed for adaptation to a changing environment in WSN.

Section –2 describes the architecture of a sensor node Section – 3 discusses the field in which FPGA is chosen for implementation of a reconfigurable Sensor Network. Section-4 describes the algorithm which is used to send the reconfiguration code to the entire network. Data Aggregation is discussed in section-5 which plays a role in power management. The proposed work is summarized in Section-6. The paper concludes with the brief discussion in Section-7.

2. Sensor node

The proposed system provides flexibility and adaptability by including a reconfigurable Hardware FPGA. The main functions of the sensor node can be classified as processing, sensing and communication tasks. The node should be made as energy efficient as possible. The nodes run in a cooperative manner for a single application or a few related applications. The tasks include sensing the physical

environment and processing of sampled data. Few Nodes can be selected as sink nodes to which all the sensor nodes report their data. This sink node plays a role in controlling the operation of sensor nodes by passing the reconfiguration information. Sink node also serves as a gateway to users and it can also act as a gateway to other networks.
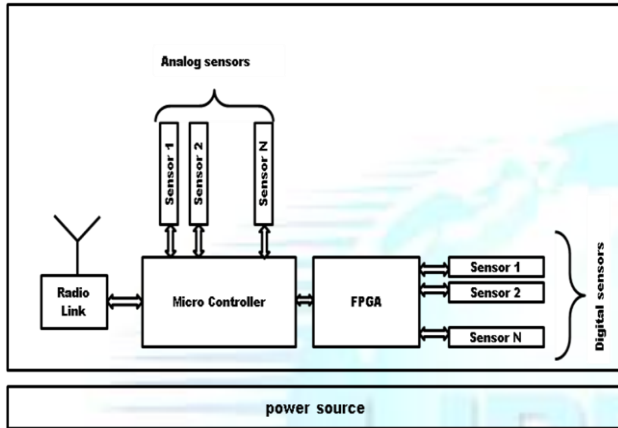

Fig. 1. Sensor node architecture

In Fig1, the architecture of the nodes is shown. Microcontroller is the heart of the system and it supports peripherals for Analog to Digital conversion. The computational task of the system includes processing of locally sensed information and the information obtained from other sensor. Microcontroller with inbuilt analog to Digital converter performs digital conversion, filtering, Processing and communication with the monitoring station.

Sensor Block includes elements which are intended to take measurement from the environment. For Multi modal sensing several sensors are present on board. The sensors of a reconfigurable node can be categorized into analog and digital sensors. Signals which are obtained from analog sensors are connected to the ADC of the microcontroller. Digital Sensors send signals to the FPGA, and they have sensors with digital interfaces.

Microcontroller in the system acts as a master device and sends control signals to the FPGA. This will activate the appropriate sensor interface. The processing of data obtained from the digital sensors will be performed by the micro controller. The analog sensors will be continuously sensing and sending the data to the node, while the digital sensors can be controlled through some reconfiguration code disseminated throughout the network. By this the system is made energy efficient. ZigBee module is used for communication between the nodes for transmission,

reception of data and Passing the reconfiguration code. Microcontroller acts as a configuration controller that takes care of loading the dynamic modules.

3. FPGA as a Reconfigurable Device

The proposed Reconfigurable Platform provides flexibility for variety of sensors and support dynamic node changes and dynamic task allocation. FPGAs are used for rapid prototyping. They can be configured many times. To solve the task of substitution and input/output management, this configuration needs a main module for controlling the tasks. Microcontroller serves this purpose. With FPGA it is possible to save resources like output Pins and energy because of outsourcing configuration data.

3.1 Need for Reconfiguration

Reconfiguration is an effective and economic solution to the changing demands in the application domain of WSN. The functionality enclosed in the system can be altered relatively simply and quickly. In expected scenarios reconfigurability is used in optimization for foreseen situations and corresponding tasks. In some unexpected scenarios it helps in adapting   the functionality of the system to the new situation. Power management is a critical issue.
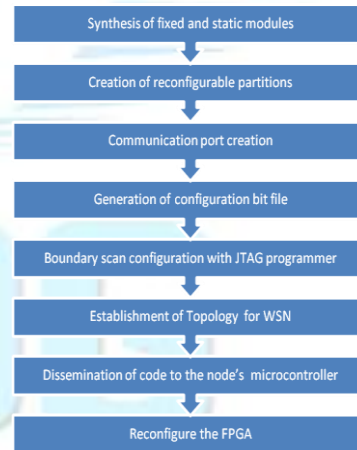

Fig. 2 Work flow of Reconfiguration

Fig 2 shows the work flow in the process of reconfiguration. The process starts with defining the reconfiguration paramaters followed by implementation through code. After that boundary scan file is created. After the establishment of definite tree topology the file is sent throughout the network starting from the sink node. The code which is sent is now received by all the nodes in the network and stored in the controller .The controller will act as a master device and

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send reconfiguration information to the FPGA connected to it. Network dynamics will have impact on the performance of the wireless sensor network. This approach has an effect on dynamic events and thereby can improve the performance of network. Reconfigurable sensor network can utilize the network efficiently. Reconfigurable systems provide high flexibility as they can be updated after system deployment and through this it can achieve time to market reduction. FPGA can reduce the tasks of controller by carrying out all the processing related to digital sensors. Hence the microcontroller can do the task of node communication and processing data from analog sensors. FPGA will send the results to the microcontroller.

3.2 Runtime reconfiguration

Modification in the functional configuration can be done even when the device is in operating mode. This feature is present in FPGAs which enables us to do runtime reconfiguration. This can be achieved using software by reconfiguring a portion of design with a new bit stream. This approach is used in military, consumer applications and communication for reducing power consumption and component cost. Xilinx FPGA offers partial reconfigurable solution. Reconfiguration regions will be present in FPGA. For making changes in the functionality in the device, bit stream should be created. This enables us an uninterrupted operation for the system.

The reconfiguration of FPGA can be actually carried out in two different ways.

When the configuration requirement of the system is a critical parameter, Run time reconfiguration is preferred. In this approach, the functionality has to be altered when the device is in operating state. Limited hardware resources in wireless terminals can be optimally used when the modification is done according to the environmental conditions. The main advantage of this approach could be the reduction in power consumption, only the required circuits are used in the FPGA. Reconfiguration is essential for future applications which require adaptability and flexibility in hardware.

3.3 Implementing a Reconfigurable system

A Bit file should be generated for making modification in the FPGA. The logic in the FPGA can be classified into two types, Static logic and Reconfigurable logic. Several bit files can be generated according to the requirements and this can be downloaded to the Reconfigurable portion of FPGA.

The fixed portion of the FPGA could be used in the external access to microcontroller and the sensors connected. Reconfigurable portion can be subdivided based on requirements. As the work of WSN lies in sensing, processing and communication of data, slots division can be done on the basis of this. First slot is dedicated for the communication with the micro controller. Slot 2 is dedicated for the processing work. Complex processing algorithms can be used with the data collected from the node. However, this feature allows us to process the data in an energy efficient way. Macros are used as a communicating module. Defining the reconfigurable module bit generation is done. The bit stream contains location information for a logic on a device including the placement of CLB, IOB and routing elements .when downloaded to a device, a bit stream configures the logic of a device and programs the device to a new desired option, which is defined through bit file.

Plan Ahead is a tool provided by Xilinx for reconfiguration. It provides a graphical user interface to deal with several options. Using Plan Ahead signals can be routed without using bus macros for communication between the created modules.FPGA editor tool is a graphical application which can be used for displaying and configuring FPGAs. After the synthesis of the design FPGA editor can be accessed. Components can be selected by clicking on item list. FPGA editor tool screen shot for digital sensor with processing part assigned to the second slot which performs the function of averaging filter. The number of occupied slices, input LUTs, bonded IOBs latches, Gclks, cell usage, Flipflop usage, Gate count and memory can be obtained from the Device utilization summary. Peak memory usage for different bit files can be compared by using the tool.
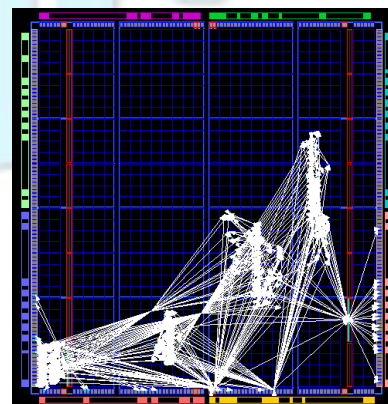

Fig. 3. View of FPGA with Xilinx planAhead tool with slots defined for controller interface,processing,sensor interface

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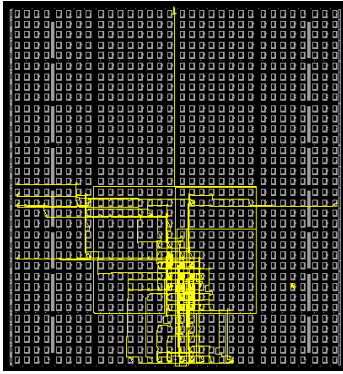ISSN: 2320 - 8791
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Fig. 4. View of FPGA Editor tool after partitioning and interfacing with a digital sensor with the data processing function of averaging filter .

Initial configuration model was developed for the application of FPGA with two digital sensors.The processing part does the function of averaging filter.Table 1 shows the details of Device utilization summary for the selected Device : 3s400pq208-5. In the similar way details can be obtained for different applications with different sensors and processing algorithms. Active CLBs can be viewed with editor tool. This shows the possibility of minimizing hardware resources for particular applications.

Table 1: FPGA Virtual Architecture Device utilization for a application with two sensors with processing function as averaging filter

Number of Slices	65
Number of 4 input LUTs	132
Number of IOs	51
Number of bonded IOBs	34 out of 141
Number of BRAMs	2 out of 16
Number of GCLKs	1 out of 8
Number of RAMB16s	2 out of 16
# Multipliers	7
Counters	10
Registers	498
Latches	28

4. Code Dissemination

The main aim of the proposed work is to achieve reconfiguration without human intervention at the deployment site. In a network, the code updates should reach all the nodes with minimum time. This could be achieved using suitable algorithm. The algorithm ensures reliability and efficiency of the whole network. The configuration code could reach all the nodes which are at multihop distance from the gateway node.

Code dissemination algorithm normally uses the concept of advertising or broadcasting. During advertisement mechanisms when the nodes in the network request for the data ,code updates will be sent to all the nodes. Delayed subscriptions can create problems with the code dissemination.

In a network where the changes in topology is always expected ,the system should be aware of the changes and make reconfiguration decisions for shifting to new tasks. Client server approach is normally used which cannot adapt automatically with unexpected changes. For stable network connectivity, periodic client Server communication requires more energy for radio communication and may result in longer delay period. Predefined events usually have the impact on performance of WSN by switching between various modes which is defined at design time. However extended service is needed for battery powered WSN which requires some changes other than low power hardware designs based on fixed hardware platforms. The configuration data is changed when the parameters are propagated into the network. The network which is already placed is changed with its parameter, hence the configuration becomes dynamic.
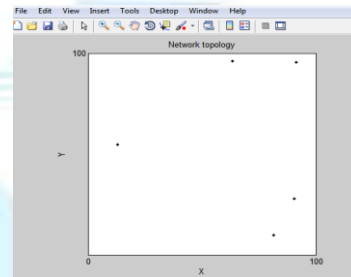

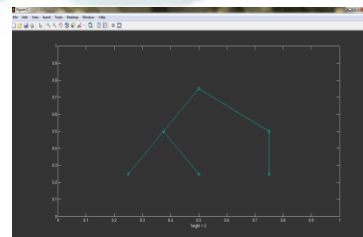Fig. 5. Random Topology for WSN for a set of five nodes using matlab tool

Fig. 6. Tree Topology for WSN after Topology Establishment phase for a set of five nodes using matlab tool

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Definite topology is absolutely necessary for the reliable code dissemination and gathering. Tree topology is chosen which can suit large networks. Implementation of Topology is shown using Matlab tool in fig 6 .This is formed from the random topology as shown is fig.5. Failure of the network will not occur even when a link between two nodes is broken. Expansion of network is also made possible by tree topology. The sink will work as the root of the tree. The process is initiated by sending the Topology Establishment Object (TEO), which contains information of the code.

Broadcasting of TEO is done by the nodes receiving it and it replies back to the sink. The parent node will have the information about the children. Once definite tree topology is formed, code updates are sent from the root(sink). Intermediate nodes forward the packet and replies to parent node for acknowledgement. Reprogramming occur after successful code dissemination. The Protocol is made fault tolerant by detecting the failed nodes. When the parent node fails, failure notification is sent to all the nodes and new parent is selected. If a node fails after receiving incomplete code, failure notification is sent along with code information. New parent is chosen from its response. The code normally follows the exact path formed by the process of the topology establishment and the complete code is passed to the entire network in the reliable way.

5. Data Aggregation

To meet the application requirements wireless sensor networks should be incredibly low power. This ultra low power operation can only be achieved by the combination of low power hardware and low duty cycle operation. Radio communication has a significant part in node's energy consumption. Protocols which are used will be designed to reduce radioactive communication. To achieve this, data should be gathered in an energy efficient manner. The idea is to combine data from different sources in such a way that it has minimal transmissions and hence energy is saved.

The tree formed during topology establishment can serve as a aggregation tree in which sink acts a root and source nodes will act as leaves. Each node will have a parent node to which the child node forwards its data. Dataflow will start from leaves node and it will be collected at the sink node. Aggregation of data is performed by parent nodes. Hence instead of transmission of data by every individual node to the sink, the parent nodes will collect the data.

6. Summary

Reconfigurable solution for WSN is proposed. FPGA is used as a separate device in the system instead of embedding a controller in it. Due to the increase in use of complex data processing algorithms,FPGA based solution can have very short execution time when implemented on it.

Tree based algorithm is implemented using Matlab tool for a set of five nodes. Sink node will act as a root node from which information is sent to all the nodes. Execution time for topology establishment and code dissemination is calculated using the tool. FPGA reconfiguration time can be calculated in real time hardware implementation. FPGA editor tool can be used in getting the graphical view of configured blocks in FPGA and the same is included. These systems can be customized based on the operating conditions. The target device selected is Spartan 3 .The framework is based on JTAG standard and this solution is portable to other FPGAs when required. The presented system uses wireless communication module based on Zigbee standard. The system can be used in particular field of application by the choice of sensors.

7. Conclusion and Future work

The proposed work can be used in WSN application fields where the system is expected to be flexible with ultra low operation. As the technology of WSN has potential for numerous applications, flexibility becomes essential in improving the performance. Control of network is made possible without need to physically reach the deployment site. The updates used are essential in achieving new functionalities. Real time implementation is possible using FPGA, microprocessors, analog sensors, digital sensors and communication module. PC can be made as a server in the reconfiguration process and the desired data can be collected from the network in an efficient way with power management strategies. Algorithms used in reconfiguration aim at reliable updating mechanism and aggregation aim at reduction in power consumption. At the pc side, application can be build for collecting data and sending commands from the server.

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